DETAILED ACTION

1. This office action is I response to the Application 10/709,665 filed 05/21/2004, amendment filed 07/02/2008 and telephone interview on 10/22/2008.

2. Claims 1-3, 5-10, 12-15 remain pending in the Application.

3. Applicant's arguments have been fully considered and are persuasive.

EXAMINER'S AMENDMENT

4. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

5. Authorization for this examiner's amendment was given in a telephone interview with Winston Hsu (Registration No. 41,526) on 10/22/2008.

6. The application has been amended as follows:

To claims

Cancel claims 5 and 12.

Claim 1 line 7 after "area" insert --, wherein the sub-circuit cells in different positions are for implementing input/output (I/O) circuit with different I/O functions--

Claim 6 line 1 after "claim" delete "5" insert --1--

Claim 7 line 1 after "claim" delete "5" insert --1--

Claim 8 line 1 after "claim" delete "5" insert --1--

Claim 9 line 13 after "functions" insert --, wherein the connection layer implements input/output (I/O) circuits with different I/O functions by the sub-circuit cells in different positions--

Claim 13 line 1 after "claim" delete "5" insert --9--

Claim 14 line 1 after "claim" delete "5" insert --9--

Claim 15 line 1 after "claim" delete "5" insert --9--

Allowable Subject Matter

7. Claims 1-3, 6-10, 13-15 are allowed.

8. The following is an examiner's statement of reasons for allowance: The prior art of record does not teach or suggest forming a plurality of input/output sub-circuits cells with the same layout in different positions of the chip, where each sub-circuit cell comprising a plurality of sub-circuit blocks and a transmission terminal, each sub-circuit block comprises at least two N-type MOS transistors or P-type MOS transistors which have doped regions with different areas, wherein the sub-circuit cells in different positions require different circuit functions, performing a layout programming in at least a connections layer so that different layouts are formed in different positions of the connection layer corresponding to the sub-circuit cells among with all limitations of the claims 1 and 9.

9. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Nation et al. (US Patent 7,043,703) discloses an apparatus comprising one or more I/) cells, one or more hard macros and one or more I/O affinity regions, which might be customized, including configuration of I/O cells by customizing diffused patterns (e.g., by metal layers) (abstract; col. 3, ll.1-4), but lacks forming a plurality of input/output sub-circuits cells with the same layout in different positions of the chip, where each sub-circuit cell comprising a plurality of sub-circuit blocks and a transmission terminal, each sub-circuit block comprises at least two N-type MOS transistors or P-type MOS transistors which have doped regions with different areas, wherein the sub-circuit cells in different positions require different circuit functions, performing a layout programming in at least a connections layer so that different layouts are formed in different positions of the connection layer corresponding to the sub-circuit cells among with all limitations of the claims. Wingren et al. (US Patent 6,823,502) discloses a tool for designing an integrated circuit that generates correct RTL for I/O beffer structures in consideration of the requirements of diffused configurable I/O blocks and/or I/O hard macros (abstract), wherein the I/O buffer structure generation tool can operate in an incremental mode, considering one additional request for an I/O buffer structure or a small change to the I/O resources of the slice, or it can operate globally, considering not only all of the I/O buffers structures, diffused configurable I/Os, hardmacs I/O, if any, but functions and blocks other that the I/O of the semiconductor product (col. 4, ll.50-56), but lacks forming a plurality of input/output sub-circuits cells

with the same layout in different positions of the chip, where each sub-circuit cell comprising a plurality of sub-circuit blocks and a transmission terminal, each sub-circuit block comprises at least two N-type MOS transistors or P-type MOS transistors which have doped regions with different areas, wherein the sub-circuit cells in different positions require different circuit functions, performing a layout programming in at least a connections layer so that different layouts are formed in different positions of the connection layer corresponding to the sub-circuit cells among with all limitations of the claims. Yeung et al. (US Patent 6,335,636) discloses a programmable I/O circuit for a programmable logic device (abstract), wherein I/O circuits is implemented using NMOS or PMOS transistors (col. 3, ll.23-30), but lacks forming a plurality of input/output sub-circuits cells with the same layout in different positions of the chip, where each sub-circuit cell comprising a plurality of sub-circuit blocks and a transmission terminal, each sub-circuit block comprises at least two N-type MOS transistors or P-type MOS transistors which have doped regions with different areas, wherein the sub-circuit cells in different positions require different circuit functions, performing a layout programming in at least a connections layer so that different layouts are formed in different positions of the connection layer corresponding to the sub-circuit cells among with all limitations of the claims.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to HELEN ROSSOSHEK whose telephone number is (571)272-1905. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

HR
10/24/2008

/Helen Rossoshek/
Primary Examiner,
Art Unit 2825